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REMARKS/ARGUMENTS

In the Office Action, the Examiner allowed claims 4, 14, 15, 19, 20, 24, 25, 29 and 30; and rejected claims 1-3, 5-13, 16-18, 21-23, 26-28, 31, and 32 under 35 U.S.C. 103(a) as being unpatentable over some combination of *LaBerge* (U.S. Pat. No. 6,108,778), *Lange* (U.S. Pat. No. 6,055,598), *Stewart* et al. (U.S. Pat. No. 6,687,773), and what was well known in the art, as exemplified by *Luo* et al. (U.S. Pat. No. 6,265,885). The Applicants appreciate the indication of allowable subject matter. Applicants traverse the rejections for the reasons set forth below. Reconsideration is respectfully requested based on the remarks below.

Claims 1, 11, 21, and 31 have been amended to further clarify the subject matter regarded as the invention. New claims 33-44 have been added. Accordingly, claims 1-44 are now pending in this application.

CLAIM REJECTIONS UNDER 35 USC 103(a)

Amended claim 1 is directed to a method for handling resets at a bus bridge. The method includes among other things the limitation of "responding to a transaction from the master component to the slave component with a bus protocol compliant signal after the reset signal is received, wherein responding with the bus protocol compliant signal allows the master component to continue operating without violating bus protocols while the slave component is being reset." Amended claims 11, 21, and 31 also recite similar limitations in their corresponding claim formats. Support for the amendments can be found in the specification on page 6, lines 15-25; page 17, lines 13-18; original claim 21; and elsewhere in the specification.

In the Office Action, the Examiner admitted that "*LaBerge* does not teach said responding with said bus protocol compliant signal allows the master component to continue operating while the slave component is being reset." (See Office Action page 3, line 20-21) The Examiner also stated that *Lange* discloses a command retrying mechanism that performs the step of responding with a bus protocol compliant signal (i.e., RETRY signal). It is respectfully submitted, however, that the RETRY signal is not a bus protocol compliant signal in the manner claimed. In particular, *Lange* does not teach or suggest that the RETRY signal allows the master component to continue operating without violating bus protocols *while the slave component is being reset*." The Examiner cited portion of col. 8, lines 19-28, in *Lange* does not disclose anything remotely to resetting a slave component. In fact, nowhere in *Lange* is there any mention that the command retrying mechanism, much less the RETRY signal, is operable in the context of a resetting event. Therefore, it is respectfully submitted that claims 1, 11, 21, and 31 are patentably distinct from the cited art.

Nonetheless, there is no motivation to combine the teachings of *Lange* with the teachings of *LaBerge*. This is because *LaBerge* teaches away from allowing the master component to continue operating, much less having it operate without violating bus protocols while the slave component is being reset. *LaBerge* discloses a device for blocking bus transactions during reset. (See Title) *LaBerge* states "it is desirable that a processor or other requesting agent be prevented or blocked from issuing a transaction on the host bus to a target agent while the target agent is in reset." (See column 1, lines 27-43) This desire is emphasized again in column 6, lines 49-62. In other words, *LaBerge* teaches preventing or blocking the master component from operating during reset. Furthermore, the command retrying mechanism and the RETRY signal are unlikely to work with the device (as disclosed in *LaBerge*) for blocking bus transactions during reset. This is because there is no indication in *Lange* that the command retrying mechanism and the RETRY signal are adapted for a resetting event. As such, there is no motivation to combine the teachings of *Lange* with the teachings of *LaBerge* in rejecting claims 1, 11, 21, and 31.

The Examiner's rejections of the dependent claims are respectfully traversed. However, to expedite prosecution, all of these claims will not be argued separately. Claims 2, 3, 5-10, 12, 13, 16-18, 22, 23, 26-28, and 32 each depend either directly or indirectly from independent claims 1, 11, 21, or 31 and, therefore, are respectfully submitted to be patentable over cited art for at least the reasons set forth above with respect to claims 1, 11, 21, or 31. Further, the dependent claims require additional elements that when considered in context of the claimed inventions further patentably distinguish the invention from the cited art.

For example, claims 16 and 26 recite the limitation of "wherein both the components are implemented in programmable logic. For example, both the master component and the slave component are implemented in programmable logic. (See page 22, line 23 to page 23, line 11 of the specification for examples of programmable logic) This is in contrast to the Examiner's reference in the Office Action on page 3, lines 8-9, to "PCI transactions being based on a configuration of programmable configuration spaces."

NEW CLAIMS

New claims 33-44 are believed to be patentable over the art of record for much the same reasons as claims 1, 11, and 21. Claims 33 and 37 include similar limitations of "wherein either the master component or slave component is implemented in programmable logic on a programmable device." Claim 41 includes a limitation of "wherein the bus bridge is implemented on a programmable device." Claims 34, 38, and 42 include similar limitations of "wherein the programmable device is selected from the group consisting of a PLD, a PLA, a PAL, a FPGA, and a CPLD." Claims 35, 39, and 43 include similar limitations of "wherein responding with a bus protocol compliant signal allows the master component to continue operating without stalling while the slave component is being reset." Claims 36, 40, and 44 include similar limitations of "wherein responding with a bus protocol compliant signal allows the master component to continue operating without locking up while the slave component is being reset."

Support for the new claims 33, 34, 37, 38, 41, and 42 can be found in the specification on page 8, line 22 to page 9, line 6; page 11, lines 3-18; page 22, line 23 to page 23, line 11; and elsewhere in the specification. Support for the new claims 35, 36, 39, 40, 43, and 44 can be found in the specification on page 6, lines 15-25; page 17, lines 13-18; and elsewhere in the specification.

SUMMARY

It is respectfully submitted that all pending claims are allowable and that this case is now in condition for allowance. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below. If any fees are due in connection with the filing of this Amendment, the Commissioner is authorized to deduct such fees from the undersigned's Deposit Account No. 500388 (Order No. ALTRP089).

Respectfully submitted,
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